Efficient Thermoelectric Cooling for Mobile Devices

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***Abstract*—Mobile apps suffer large performance degradation when the underlying processors are throttled to cool down the devices. Fans or heat sinks are not a viable option for mobile devices, thus calling for a new portable cooling solution. *Thermoelectric coolers* are scalable and controllable cooling devices that can be embedded into mobile devices on the chip surface. This paper presents a thermoelectric cooling solution that enables efficient processor thermal management in mobile devices. Our goal is to minimize performance loss from thermal throttling by efficiently using thermoelectric cooling. Since mobile devices experience large variations in workloads and ambient temperature, our solution adaptively controls cooling power at runtime. Our evaluation on a smartphone using mobile benchmarks demonstrated that the performance loss from the maximum speed is only 1.8% with the TEC compared to 19.2% without the TEC.**

I. Introduction

Mobile devices such as smartphones, tablets and laptops have become a primary computing/communication platform due to their portability and high computational power. In turn, processor chips thereon must cope with dangerously high temperature with their limited cooling capability [1]. Since using a fan or heat sink is not a viable solution, mobile devices rely on *thermal throttling* such as voltage/frequency scaling. When a given temperature threshold is reached, mobile devices are cooled down by reducing the processor speed, thus applications thereon experience significant lagging. In particular, interactive mobile applications that require real-time responsiveness suffer from large performance degradation.

Thermoelectric coolers (TECs) are compact and controllable cooling devices that actively extract heat by flowing cooling current via *Peltier effect* [2]. Recent studies suggest that thin-film TECs can meet the cooling demand of modern microprocessors [3]. Since TECs can be built in a micro scale (13mm^3 footprint), they can be embedded into mobile devices while conventional cooling hardware cannot fit into the device form factor. Also, unlike cooling fans, solid-state TECs are reliable and noise-free, making them an attractive cooling solution for mobile devices.

Existing proposals for the TEC focus on high-power desktop/server processors optimizing the *static* TEC cooling power in conjunction with fan cooling [4]–[6]. However, low-power mobile processors dissipate substantially less heat than previous analysis [6], [7], rendering the TEC a feasible cooling solution without fan. Also, unlike server systems, mobile devices exhibit large variations not only in operating ambient but also application workloads in response to sporadic user activities [8]. This paper focuses on *dynamic* control of the TEC adaptive to various runtime thermal scenarios in mobile devices.

We present thermoelectric cooling solution embedded into mobile devices on the chip surface that enables efficient processor thermal management. Our goal is to minimize performance degradation from thermal throttling by efficiently using the TEC. Our solution controls the TEC cooling power adaptively to the runtime workloads and ambient temperature.

To address this challenge, we first need to model the thermal characteristics of the TEC and the processor chip. Using the system thermal model, we then need to determine the optimal cooling current and perform adaptive cooling control by tracking runtime workloads and ambient temperature. Chip temperature forms a convex function of the cooling current and the processor speed, facilitating mathematical optimization to determine the optimal cooling current. At runtime, we read thermal sensors to learn a *processor activity factor* and adaptively control the cooling power.

We have evaluated the effectiveness of the TEC cooling solution on a smartphone using representative mobile benchmarks [9]. When running compute-intensive workloads without the TEC, the processor speed is lowered to the minimum level resulting in significant lagging. Using the TEC, the processor speed can be maintained close to the maximum speed; only reduced 1.8% on average with the TEC compared to 19.2% without the TEC. Our TEC solution achieves the maximum performance at cost of 0.2W cooling power consumption by adaptively controlling the TEC. We also perform thermal simulations to complement the experimental evaluation for extreme ambient temperatures by emulating the TEC with thermal parameters identified from the experiments. The results showed the large performance degradation under the adverse ambient can be saved by using the TEC but at the cost of higher cooling power consumption.

The main contributions of the paper are:

- Feasibility test of thermoelectric cooling for mobile devices;
- Dynamic cooling control adaptive to the runtime workloads and ambient temperature; and
- Demonstration and in-depth evaluation on a smartphone.

The rest of the paper is organized as follows. Sec. II presents the motivation of this work and Sec. III overviews the system thermal model. Sec. IV presents our thermal management solution that optimizes cooling power and adaptively controls runtime temperature. Sec. V evaluates the proposed solution using experiments and simulations. Sec. VI discusses related work. The paper concludes with Sec. VII.

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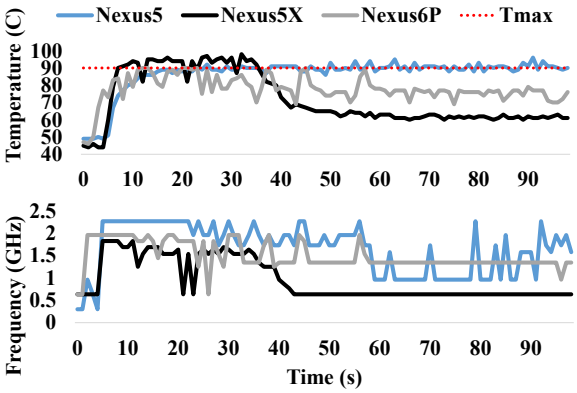


Fig. 1: Chip temperature and frequency traces from Nexus 5/5X/6P while running Mibench benchmark [10]

II. Motivation

Modern mobile devices are powered by state-of-the-art multi-core chips; Yet, they cannot leverage their computing power due to limited cooling capability without fans or heat sinks. Our measurements for Nexus 5/5X/6P smartphones in Fig. 1 show that CPU-intensive benchmark application [10] quickly raises the chip temperature beyond the specified temperature threshold within 20s, throttling processor frequency thereafter. Processor frequency is reduced to 56/35/68% of maximum speed on average, thus applications thereon suffer large performance degradation. This calls for a new portable cooling technology for mobile devices.

TECs can be used for mobile devices due to its scalable size and solid-state property. While the TEC can instantly extract heat from cold side to hot side consuming active cooling power, cooling effect is limited when the heat accumulates at the hot side. However, mobile devices only demand cooling power for short bursts of user activities and idle most of the time, and thus the heat does not continuously accumulate at the hot side. Also, mobile processors are designed with orders of magnitude smaller thermal design power (TDP) [1] to operate without fan or heat sink, thus the hot side temperature does not increase much. Instantaneous cooling of the TEC devices can efficiently cool down the processor in response to sporadic workloads, and it must be dynamically controlled according to the runtime workloads to minimize cooling power consumption.

III. System Thermal Model

Fig. 2 illustrates a TEC device that can be embedded on top of the chip packaging. We consider a processor chip tiled with TEC modules extracting heat to the external ambient. In this paper, ambient temperature is the average temperature surrounding the chip packaging affected by the heat dissipation from other components such as battery, display and communication modules. This section describes how to model the TEC cooling capacity, processor power consumption and system-level thermal behavior.

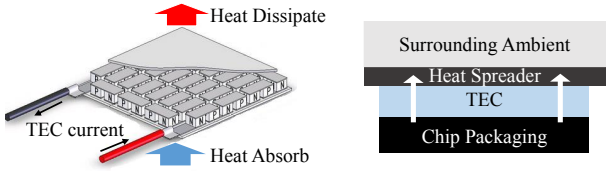
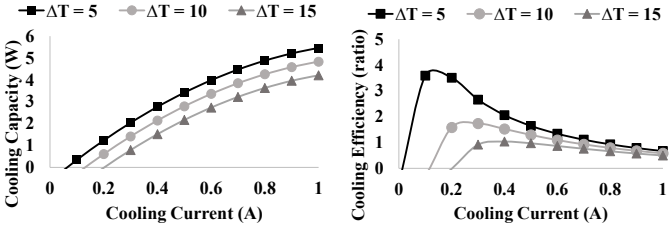


Fig. 2: TEC device and chip packaging with embedded TEC



(a) Net Cooling Capacity (b) Cooling efficiency

Fig. 3: (a) Net cooling capacity and (b) cooling efficiency of a TEC depending on temperature difference between two sides

A. TEC Cooling Model

A TEC is a solid-state device made of arrays of N- and P-type semiconductor pellets. When electric current flows through the thermoelectric material, heat is absorbed from cold side and dissipated to hot side via *Peltier effect* [2]. This thermoelectric heat pump can be controlled by the current. The amount of cooling effect on the cold side and heat dissipation on the hot side can be modeled as [4]:

$$P_c = -ST_cI_{\text{TEC}} + \frac{1}{2}I_{\text{TEC}}^2 r_{\text{TEC}} \quad P_h = ST_hI_{\text{TEC}} + \frac{1}{2}I_{\text{TEC}}^2 r_{\text{TEC}} \tag{1}$$

where S is *Seebeck* coefficient, I_{TEC} is the cooling current, T_c and T_h are the temperatures on the cold and hot sides, and r_{TEC} is the electrical resistance generating heat on both sides. The cooling power consumption is computed as [4]:

$$P_{TEC} = P_h - P_c = I_{\text{TEC}}^2 r_{\text{TEC}} + S(T_{\text{h}} - T_{\text{c}})I_{\text{TEC}}. \tag{2}$$

While active TEC cooling extracts heat from cold to hot side, heat dissipate from hot to cold side through heat conduction, thus limiting TEC cooling capacity described as:

$$P_{\text{net}} = -ST_{\text{chip}}I_{\text{TEC}} + \frac{1}{2}I_{\text{TEC}}^2 r_{TEC} + \frac{T_h - T_c}{R_{\text{TEC}}} \tag{3}$$

Fig. 3 shows the cooling capacity and efficiency of the TEC for the varied TEC current. As temperature difference (Δ T) increases, the more heat conducts to cold side, limiting the net cooling capacity. Because the TEC power consumption quadratically increases with cooling current, cooling efficiency ($\frac{P_{\text{net}}}{P_{\text{TEC}}}$) is higher with a smaller cooling current. Comparing to high-power desktop/server chips, low-power mobile chips demand a small cooling current where cooling efficiency of the TEC is maximized.

B. Processor Power Model

Processor heat dissipation can be modeled by dynamic and leakage power consumption [11]. The dynamic power

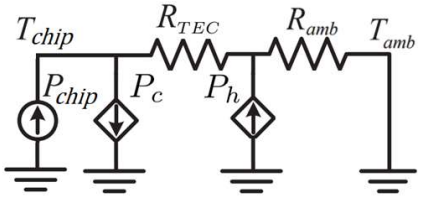
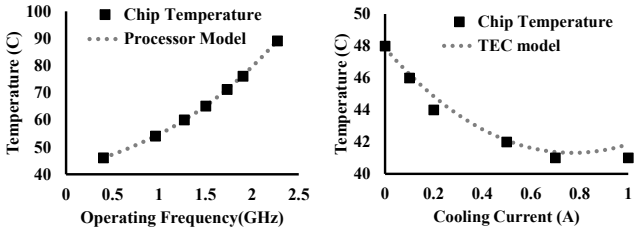


Fig. 4: Thermal circuit model of the TEC system

$T_{\text{chip}}, T_{\text{amb}}$	Chip and surrounding ambient temperatures
$P_{\text{chip}}, P_c, P_h$	Chip heat dissipation, TEC heat pump
$R_{\text{TEC}}, R_{\text{amb}}$	Thermal resistances between chip-TEC, TEC-ambient



(a) Varied processor frequency (b) Varied cooling current

Fig. 5: Thermal model identification with the varied (a) processor frequency (b) TEC current

is consumed when executing workloads depending on the processor voltage/frequency and activity caused by workloads. Leakage power is statically consumed even when processor is idle. Leakage power increases with temperature that can be approximated by a linear model [12]. The processor power consumption is equal to:

$$P_{\text{chip}} = P_{\text{dyn}} + P_{\text{leak}} = CV^2 f\alpha + V(\beta_1 T_{\text{chip}} + \beta_0) \quad (4)$$

where C is constant load capacitance, V, f are processor voltage/frequency, α is processor activity factor caused by the workloads, T_{chip} is the average chip die temperature and β_1, β_0 are leakage parameters. The leakage parameters, β_1, β_0, are platform-dependent constants depending on the technology that can be characterized at design time. Whereas the activity factor α is a runtime parameter capturing the real-time CPU workloads that must be characterized at runtime.

C. System Thermal Model

Since the TEC cooling capacity and efficiency greatly depends on the temperature difference between hot and cold sides of the TEC as shown in Fig. 3, we need a system thermal model to efficiently control the TEC. By combining TEC and processor models, Fig. 4 is the RC thermal circuit model that corresponds to the chip packaging with the TEC in Fig. 2. The TEC extracts heat from the cold side on the chip surface (P_c) to the hot side (P_h) that eventually dissipates to the ambient. In the steady-state, chip temperature can be written as:

$$T_{\text{chip}} = T_{\text{amb}} + R_{\text{amb}} P_h + (R_{\text{TEC}} + R_{\text{amb}})(P_{\text{chip}} - P_c) \quad (5)$$

While thermal resistances and the TEC thermal constants can be determined at design time via *system identification* [11], the changing ambient temperature T_{amb} needs to be captured at runtime.

IV. Processor Thermal Management

Our focus in this paper is to minimize the performance loss from thermal throttling by efficiently controlling the TEC cooling power. We first identify the model parameters to optimize the TEC cooling current. Then, we dynamically control cooling power according to runtime ambient and workloads.

A. Thermal Model Identification

To optimize the TEC, we first need to identify the thermal model parameters of the target platform. By leveraging thermal sensors available on most mobile devices [1], we can perform *system thermal identification* to learn the thermal model parameters. We run mobile benchmark workloads [10] for a long enough time and measure the steady-state chip temperature while ambient temperature remains constant. The steady-state temperature measurement is repeated for the varied processor frequency and TEC cooling current. Fig. 5 illustrates the system thermal identification using varied processor frequency and cooling current. By plugging the measured chip temperature, the processor frequency and the TEC cooling current into Eq. (5), the thermal constants and TEC parameters can be identified. Sec. V-A will provide details on the experimental setups.

Fig. 5a presents the measured chip temperature and identified thermal model at different processor frequencies without the TEC cooling. Chip temperature increases with processor frequency following the dynamic power model in Eq. (4). The measured chip temperature (plotted as square) accurately fits in the processor thermal model (plotted as dashed line) using the identified thermal parameters. Fig. 5b plots the steady-state chip temperature at the different TEC cooling currents while the processor is idle. Chip temperature cools down with increasing cooling current but Joule heat dissipation grows quadratically limiting the net cooling capacity according to Eq. (3). The TEC thermal parameters can be identified from the these measurements, and the chip temperature (plotted as square) can be well approximated by the TEC thermal model (plotted as dashed line).

The leakage parameters are also identified by placing the device under the varied ambient temperature while the processor is idle. The measured leakage power can be approximated well by a linear fitting across 45 °C to 85 °C of on-chip temperature. The identified power and thermal model parameters are summarized in Table. I.

TABLE I: Identified leakage and thermal parameters

Leakage Power		Thermal Resistance		TEC parameters	
β_1	β_0	R_{TEC}	R_{amb}	S	r_{TEC}
0.016	0.035	3.4W/K	17.4 W/K	0.022 V/K	0.5 Ω

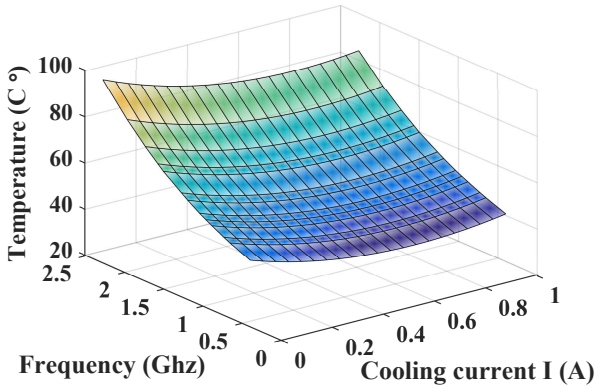


Fig. 6: Convexity of chip temperature for the varied processor frequency and TEC cooling current

B. TEC Optimization

For given processor activity and ambient temperature, we can find the optimal cooling current using the proposed thermal model. Our goal is to minimize thermal throttling while meeting the chip temperature and power constraints that can be formulated as follows:

Given runtime processor activity factor α and ambient temperature T_{amb},

Find the maximum allowed operating frequency f and the corresponding TEC cooling current I_{TEC} that meet the power and thermal constraints $P_{\text{max}}, T_{\text{max}}$.

$$\max_{I_{\text{TEC}}} \quad f \tag{6}$$

$$\text{s.t } T_{\text{chip}} \leq T_{\text{max}} \tag{7}$$

$$P_{\text{total}} \leq P_{\text{max}} \tag{8}$$

Eq. (6) defines our objective to find the maximum allowed processor frequency subject to the power and thermal constraints. Since interactive mobile applications are usually latency-sensitive, their performance directly impacted by processor speed. We aim to find the maximum allowed processor speed for real-time responsiveness of mobile applications.

Eqs. (7),(8) specify the thermal and power constraints of the platform. To guarantee maximum temperature for long-running workloads, the steady-state temperature needs to be lower than the temperature threshold. Also, the total power consumption of chip and cooling device must be lower than the power constraint.

Eq. (5) describes that the steady-state chip temperature is a convex function of processor frequency f and cooling current I. Fig. 6 illustrates the chip temperature for different processor frequency and cooling current using the identified model parameters. Due to its convexity, the optimization problem can be efficiently solved by interior point method with complexity of $O(n^{3.5})$ for typical case [13]. To avoid runtime overhead, we optimize the TEC in design time for a range of chip and ambient temperature, and online thermal control may use it via a table lookup.

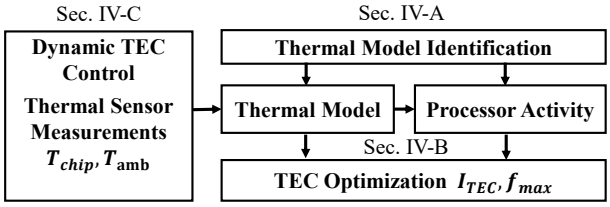


Fig. 7: Workflow diagram of dynamic TEC control

C. Dynamic TEC Control

In mobile systems, not only runtime workload but also ambient temperature dynamically changes over time. We need to adapt cooling power to runtime CPU load and operating ambient for efficient thermoelectric cooling. Modern mobile devices are equipped with on-chip and off-chip thermal sensors that can be used to learn the runtime chip and surrounding ambient temperature.

Fig. 7 shows how we learn runtime CPU workload and operating ambient using thermal sensor measurements. We measure both the on-chip and off-chip thermal sensors ($T_{\text{chip}}, T_{\text{amb}}$) and plug into Eq. (5) to calculate the processor power (P_{chip}). From the processor power model in Eq. (4), we can learn the processor activity factor (α) caused by the application workloads running on the processor. Using thus-obtained runtime thermal parameters (α, T_{amb}), we can optimize the TEC cooling current and processor frequency (I_{TEC}, f) that meet the thermal and power constraints.

This dynamic thermal management is periodically invoked to adapt to various runtime thermal scenarios. The period must be short enough to quickly react to the application workloads that may overheat the chip. Chip temperature does not increase instantly due to thermal time constant, and it requires several seconds to reach the threshold as shown in Fig. 1. Thus, the invocation period could be order of second such that the runtime overhead is low.

While our goal is to maximize performance, CPU frequency can be lowered for power savings when CPU load is low. To allow DVFS governor for power savings, we only set the maximum allowed frequency and corresponding to the TEC cooling. Thus underlying DVFS governor may adjust frequency depending on the runtime workload within the allowed range by TEC cooling.

V. Evaluation

We have experimented our TEC solution on a smartphone, and also performed extensive simulations by emulating the TEC. Thermal simulations complement the experiments allowing us to examine the extreme ambient and various workloads.

A. Experimental Setup

Our experiment was on Nexus 5 powered by quad-core Snapdragon 800 that supports chip-wide DVFS with maximum frequency of 2.26GHz. The device is equipped with on-chip and off-chip thermal sensors with 1 °C precision. We used on-chip thermal sensors to obtain average chip die temperature and off-chip thermal sensors for the surrounding ambient

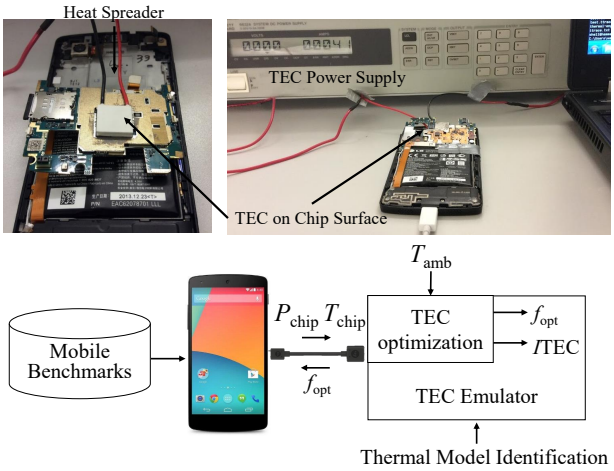


Fig. 8: Experiment and Simulation setup

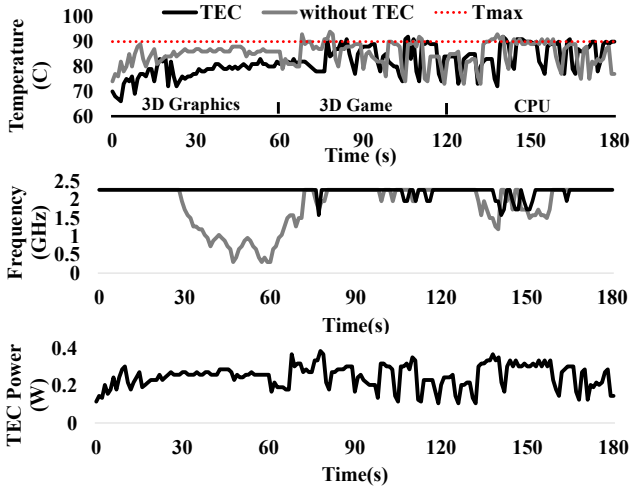


Fig. 9: Temperature, frequency and cooling current traces from the experiment running Antutu mobile benchmark [9]

temperature. For the TEC, we used CP60133 [14] with silver-based thermal paste (Arctic Silver 5) rated maximum cooling capacity of 12.2W at maximum cooling current of 6.0A. The TEC is powered by programmable power supply, HP 6632A. Fig. 8 demonstrates our experimental setup. Since processor chip is facing the front panel, we placed the TEC on the chip surface and reinstall it to the original configuration. Thus, the hot side of the TEC was facing the heat spreader on the front panel and the back cover was also reinstalled in the experiment. We used performance governor for DVFS and default thermal governor in Android kernel such that frequency is only reduced when specified temperature threshold is reached. As representative mobile workloads, we used Antutu benchmark suite v6.2 [9] comprise 3D graphics and games and multi-thread CPU operations. We also tested Mibench benchmarks [10] from 3 different categories of computational, network, communication representing typical operations in mobile systems.

We also perform simulations by emulating the TEC to examine the proposed solution for various workloads under the different operating ambient. As shown in Fig. 8, we obtain power and temperature traces from the devices while running mobile applications, and emulate the TEC using thermal parameters identified from the experiments. The simulation was done in MATLAB similar to the HotSpot thermal simulator [5].

Throughout the evaluation, we compare proposed solution with the baseline system without the TEC. We evaluate temperature control, CPU performance and power consumption of the TEC.

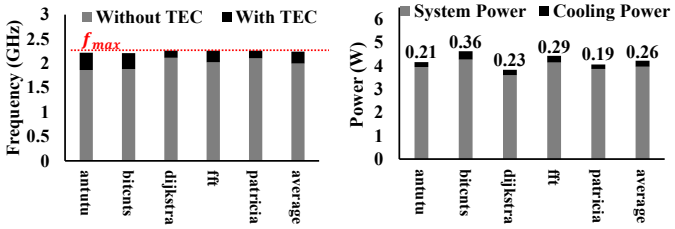
B. Experimental Results

In the experiments, we focused on dynamic thermal control and performance gain using the TEC. We run Antutu benchmark suite that runs 3D graphics, 3D gaming and CPU-intensive workloads for 3 minutes. Fig. 9 shows the real-time traces of the chip temperature, processor frequency and TEC power consumption. While processing 3D graphics, baseline without the TEC quickly reached temperature threshold and throttled the processor frequency during 30s to 75s. The processor frequency was largely reduced to minimum level, 0.3GHz, where graphics are significantly lagging. The overall processor frequency while running benchmark suite was 1.87GHz translated to 19.2% performance loss with respect to the maximum processor speed.

Proposed TEC solution could maintain the processor temperature lower than temperature threshold while maintaining processor frequency close to maximum level. In particular, large performance loss during 30s to 75s can be saved by using the TEC. The minimum processor frequency was 1.6GHz using the TEC over 0.3GHz without the TEC, thus resulting in more reliable latency for user applications. When processor heat dissipation still exceeded the cooling capacity, processor frequency is briefly lowered at around 150s. The average processor frequency was 2.22GHz translated to only 1.8% performance loss, improving 18.9% over baseline without the TEC. Our TEC solution also reduces thermal violation to 1.1% from 3.3% wihtout the TEC. It does so with dynamic TEC control consuming average cooling power of 0.21W, comparable to a Wifi module power consumption [15]. Without dynamic cooling control, the TEC must maintain worst-case cooling power of 0.39W for peak workloads, consuming 86% increased cooling power. The results demonstrate the feasibility of the TEC for mobile devices and efficiency of dynamic cooling control.

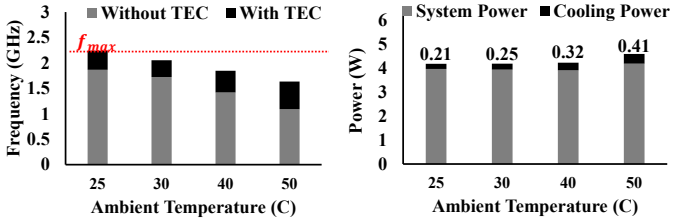
C. Simulation Results

In simulations, we focus on trade-off between performance vs. cooling power consumption across different benchmarks and ambient temperatures. Fig. 10 shows the processor frequency and total power consumption under the room temperature with and without the TEC. Note that the TEC cooling power consumption is presented on the top of the bar. Using the TEC, all the applications may run close to maximum processor frequency, 2.24GHz on average translated to 0.7% performance loss. The average cooling power consumption was 0.26W that corresponds to 6% of system



(a) Processor Frequency (b) Power Consumption

Fig. 10: (a) Processor frequency and (b) power consumption with and without the TEC for benchmark applications



(a) Processor Frequency (b) Power Consumption

Fig. 11: (a) Processor frequency and (b) power consumption with and without the TEC for different ambient temperature

power consumption. Performance improvement is especially significant for compute-intensive workloads since they suffer a larger performance degradation from thermal throttling, for example, 23.9% for *bitcnts* compared with 7.5% for *patricia*. As consequence, compute-intensive *bitcnts* demand more cooling power 0.36W for compared to 0.19W for *patricia*. Thus, the TEC system enables peak performance operations in mobile platforms that was limited by cooling capacity; however, this peak performance comes at cost of the TEC power consumption.

We also simulate different ambient temperatures for running Antutu benchmarks. At the high ambient temperature, baseline without the TEC suffer a large performance loss from thermal throttling. Without the TEC, average frequency in case of 40°C (50 °C) ambient temperature was reduced to 1.42GHz (1.09GHz) translated to 37.1% (51.7%) performance loss. Using the TEC, average frequency can be maintained to 1.84GHz (1.63GHz) translated to 18.5% (27.8%) performance loss for 40°C (50 °C). However, cooling power consumption is also increasing with higher ambient temperature of 0.41W for 50 °C. The results showed that the performance degradation under the high ambient temperature can be largely mitigated, which is especially significant for mobile devices that experience a large variations in its operating ambient.

VI. Related Work

To cope with increasing chip temperature, new cooling techniques have received significant attention in recent years. Chowdhury *et al.* [3] demonstrated that modern thin-film TECs can meet the cooling requirement of on-chip hotspot. Chaparro *et al.* aim to enhance existing dynamic thermal management using the TEC [16]. Long *et al.* [4] optimized the deployment of TEC devices and the static cooling current. Dousti *et al.* [5], [6] optimize cooling power of the fan cooler and TEC to minimize power consumption. Recent study [7] investigate energy harvesting and cooling with fan cooler on a fully instrumented TEC cooling system.

Unlike existing solutions, we aim to adaptively control the TEC not only for runtime workloads but also for the surrounding ambient temperature, which is significant for mobile devices. While previous studies focus on desktop/server processors [4], [5] rated over 80W with fan coolers [6], [7], we propose the use of TECs for mobile devices rated at most 3W of power consumption that can be efficiently cooled by small amount of cooling power consumption.

VII. Conclusion

We present a thermoelectric cooling solution for mobile devices. In particular, dynamic TEC control is proposed for efficient processor thermal management. Because mobile systems face large variations in runtime workloads and ambient temperature, our solution adaptively controls TEC using online information. Our evaluation on a smartphone has demonstrated its effectiveness in maintaining peak performance, which is especially important for interactive mobile apps. Our experimentation with realistic mobile workloads has shown an only 1.8% performance loss with TEC compared to 19.2% loss without TEC at the cost of 0.2W cooling power consumption.

Acknowledgment

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